

12bit 2 channels SAR AD converter IC**MM3804A12RLE
Datasheet****FUNCTION**

12-Bit Two Channels Successive Approximation Type Analog to Digital Converter IC.

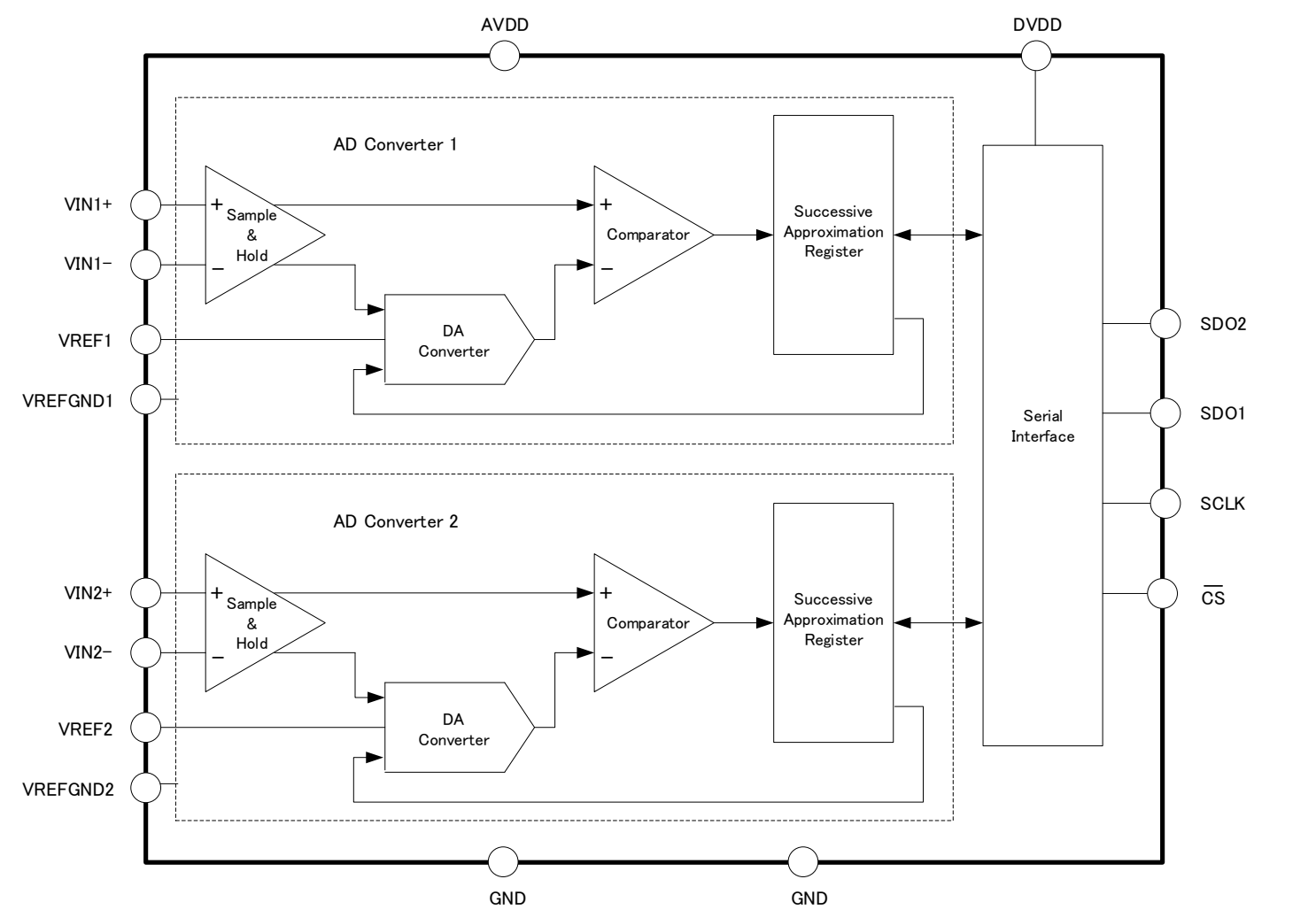
FEATURES

- High sampling rate : 750Ksps
- Pseudo differential analog inputs
- Two-channel simultaneous sampling

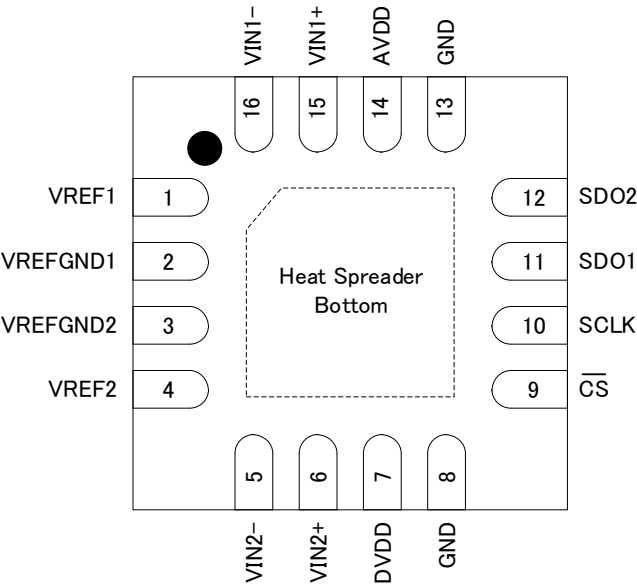
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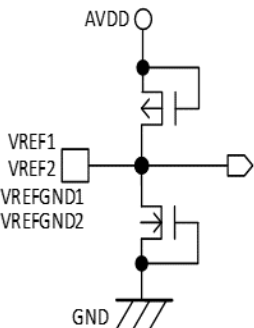
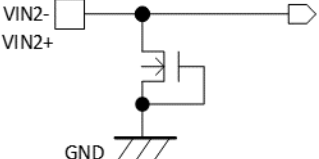
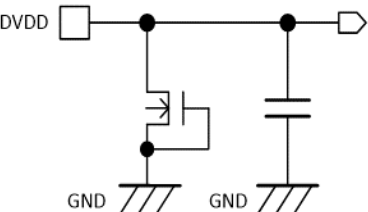
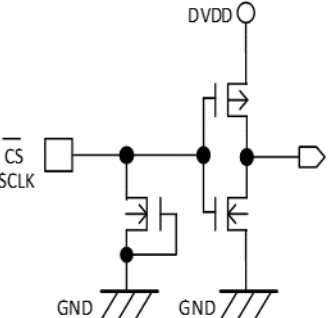
BLOCK DIAGRAM



PIN CONFIGURATION



TERMINAL EXPLANATIONS

PIN No.	SYMBOL	TYPE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
1	VREF1	Input		Reference voltage input for ADC1
2	VREFGND1	Supply		Reference voltage GND for ADC1
3	VREFGND2	Supply		Reference voltage GND for ADC2
4	VREF2	Input		Reference voltage input for ADC2
5	VIN2-	Input		Minus analog input for ADC2
6	VIN2+	Input		Plus analog input for ADC2
7	DVDD	Supply		Power supply for digital I/O
8	GND	Supply	-	Ground
9	CS	Input		Chip select input
10	SCLK	Input		Serial communication clock input

PIN No.	SYMBOL	TYPE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
11	SDO1	Output		Serial communication data output for ADC1
12	SDO2	Output		Serial communication data output for ADC2
13	GND	Supply	-	Ground
14	AVDD	Supply		Power supply for ADC
15	VIN1+	Input		Plus analog input for ADC1
16	VIN1-	Input		Minus analog input for ADC1

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	AVDD DVDD	-0.3	7.0	V
Analog input voltage	(note ¹)	GND-0.3	AVDD+0.3	V
Digital input voltage	(note ²)	GND-0.3	DVDD+0.3	V
Ground voltage difference	GNDd	-	0.3	V
Storage temperature	Tstg	-65	150	deg.C
Power dissipation (On board)	Pd	-	2.7	W

note¹: VIN1+, VIN1-, VREF1, VIN2+, VIN2-, VREF2

note²: CS, SCLK,SDO1,SDO2

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating ambient temperature	Top	-40	-	125	deg.C
AVDD operating voltage	AVDDop	4.5	5	5.5	V
DVDD operating voltage	DVDDop	1.65	3.3	5.5	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25deg.C, AVDD=5V, DVDD=3.3V, VREF1=VREF2=2.5V, Sampling rate (fsample) = 750Ksps)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
Analog supply current (operational)	Iavop	AVDD=5V, fsample=750ksps	-	6.0	7.0	mA
Analog supply current (static)	Iavst	AVDD=5V, CS=H	-	4.0	6.0	mA
Digital supply current	I _{dv}	DVDD=3.3V fsample=750ksps	-	0.20	-	mA
Analog input						
Full-scale input range	FSR	(note ³)	-Vref	-	Vref	V
Absolute input voltage (+)	Vin+	(note ³)	0.0	-	2 × Vref	V
Absolute input voltage (-)	Vin-		Vref-0.1	Vref	Vref+0.1	V
Input capacitance (note ⁴)	Cina	Sample mode	-	15	-	pF
		Hold mode	-	4	-	pF
Input leakage current	Iina		-	1.5	-	nA
Reference voltage input						
Reference input voltage	Vref		2.25	2.5	AVDD/2	V
Current drain	Iref		-	300	600	μA
	Irefl	CS=AVDD	-	0	1	μA

note³: Each of the following conditions is required to use this IC with the maximum dynamic range.

FSR_ADC1 = 2 × VREF1, FSR_ADC2 = 2 × VREF2

VIN1+ = 0 to 2 × VREF1, VIN2+ = 0 to 2 × VREF2

ViIN1- = VREF1, ViIN2- = VREF2

AVDD ≥ 2×VREF1, AVDD ≥ 2×VREF2

note⁴: Specified by design

(Unless otherwise specified. Ta=25deg.C, AVDD=5V, DVDD=3.3V, VREF1=VREF2=2.5V, Sampling rate (fsample) =750Ksps)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution						
Resolution	Reso		-	-	12	Bits
Sampling dynamics						
Data rate	fsample		-	-	750	Ksps
Aperture delay (note ⁵)	tap		-	4	-	ns
Clock frequency	f _{clk}		-	-	24	MHz
DC accuracy						
Integral nonlinearity	INL		-2	-	2	LSB (note ⁶)
Differential nonlinearity	DNL		-1	-	2	LSB
Input offset error	Vof		-2	-	2	LSB
Input offset thermal drift (note ⁵)	dVof/dt		-	0.01	-	LSB /deg.C
Gain error	Gerr	Refers to the voltage of VREF1 and VREF2.	-4	-	4	LSB
Gain error thermal drift (note ⁵)	Gerr/dt	Refers to the voltage of VREF1 and VREF2.	-	0.004	-	LSB /deg.C
Common mode rejection ratio	CMRR	Signals of DC to 20kHz are input to ADC1 and ADC2.	-	70	-	dB

note⁵: Specified by design

note⁶: When VREF is 2.5V, 1 LSB is 1.22mV.

(Unless otherwise specified. Ta=25deg.C, AVDD=5V, DVDD=3.3V, VREF1=VREF2=2.5V, Sampling rate (fsample) =750Ksps)

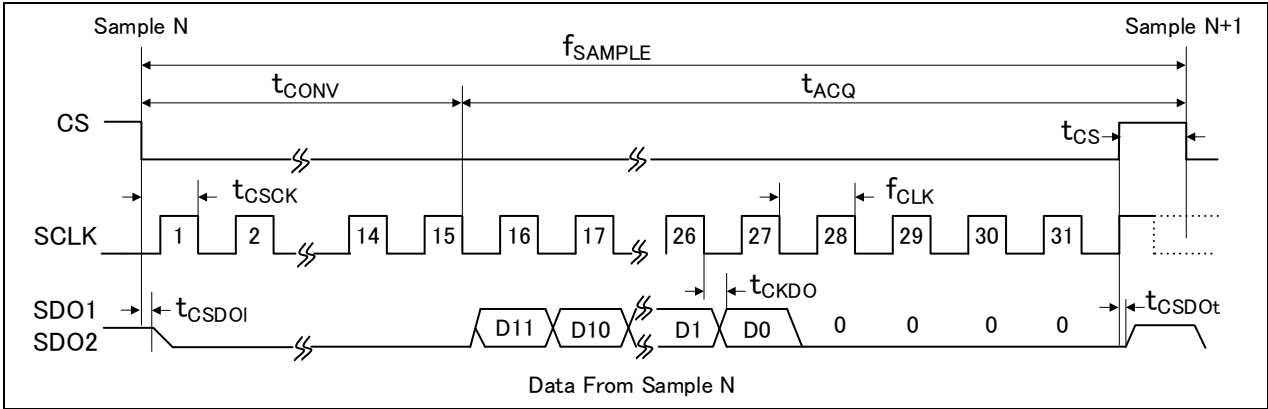
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AC accuracy						
Total harmonic distortion	THD	-0.5dB [full scale] at 20kHz input	-	-76	-	dB
		-0.5dB [full scale] at 100kHz input	-	-75	-	dB
		-0.5dB [full scale] at 250kHz input	-	-72	-	dB
Signal to (noise + distortion) ratio	SINAD	-0.5dB [full scale] at 20kHz input	-	70	-	dB
		-0.5dB [full scale] at 100kHz input	-	69	-	dB
		-0.5dB [full scale] at 250kHz input	-	67	-	dB
Signal to noise ratio	SNR	-0.5dB [full scale] at 20kHz input	-	71	-	dB
		-0.5dB [full scale] at 100kHz input	-	70	-	dB
		-0.5dB [full scale] at 250kHz input	-	68	-	dB
Spurious free dynamic range	SFDR	-0.5dB [full scale] at 20kHz input	-	78	-	dB
		-0.5dB [full scale] at 100kHz input	-	77	-	dB
		-0.5dB [full scale] at 250kHz input	-	74	-	dB
Isolation between ADC1 and ADC2	Iso12	f _{IN} =15kHz, f _{NOISE} =25kHz	-	-85	-	dB
Full power bandwidth	BW _{FP}	-3dB	-	25	-	MHz
		-0.1dB	-	5	-	MHz
Digital input (note ⁷)						
High level input voltage	V _{IH}		0.7× DVDD	-	DVDD +0.3	V
Low level input voltage	V _{IL1}	DVDD≥2V	-0.30	-	0.3× DVDD	V
Low level input voltage	V _{IL2}	DVDD<2V	-0.30	-	0.15× DVDD	V
Digital output (note ⁷)						
High level output voltage	V _{OH}	I _{oh} =500μA source	0.8× DVDD	-	DVDD	V
Low level output voltage	V _{OL}	I _{ol} =500μA sink	0	-	0.2× DVDD	V

note⁷: Specified by design

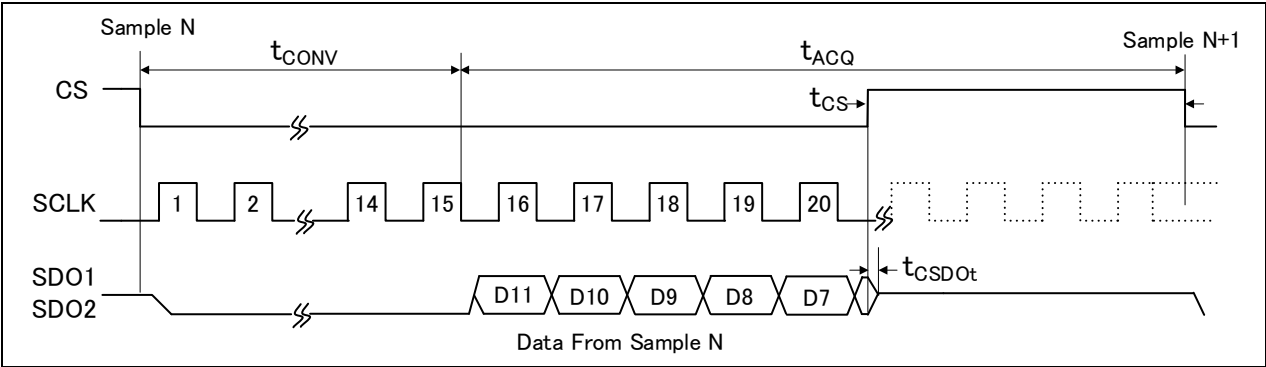
TIMING CHARACTERISTICS

(Unless otherwise specified. Ta=25deg.C, AVDD=5V, DVDD=3.3V, VREF1=VREF2=2.5V, Sampling rate (fsample) =750Ksps)

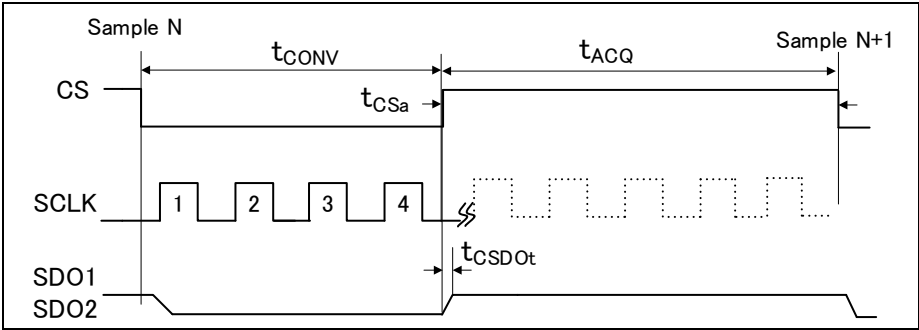
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data rate	fSAMPLE		-	-	750	Ksps
Clock frequency	fCLK		-	-	24	MHz
Clock duty	Duty		40	-	60	%
Conversion time	tCONV		-	-	15	clock cycles
Acquisition time	tACQ	fck=24MHz	70	-	-	ns
CS high time	tCS		20	-	-	ns
CS high time after frame abort	tCSa		70	-	-	ns
SCLK setup time	tCSCK		15	-	-	ns
SDO Delay time	tCKDO		3	-	20	ns
SDO tristate delay time 1	tCSDOI		-	-	12	ns
SDO tristate delay time 2	tCSDOt		-	-	10	ns



· Normal Conversion timing diagram



• Short cycle read timing diagram



• Abort timing diagram

Fig. 1 Analog to digital conversion timing diagram

DETAILED DESCRIPTION

OVERVIEW

MM3804A12 is a successive approximation type of AD converter IC, which can simultaneously convert two analog signals to 12-bit data at 750 Ksps at the maximum. This IC supports pseudo-differential input of analog signals. SPI is used for communication with an external digital host.

ANALOG TO DIGITAL CONVERSION

Fig. 2 shows a timing diagram. MM3804A12 requires a minimum of 26-SCLK falling edge between CS falling edge and CS rising edge to perform 12-bit analog to digital conversion. The conversion is started from the CS falling edge, and the sampled analog values are converted to digital values during 15 SCLKs. The values output from SDO1 and SDO2 are "0" during this conversion period.

The sample and hold circuit returns to the sampling mode at the 15th SCLK falling edge. Moreover, the MSBs of ADC1 and ADC2 are output to SDO1 and SDO2 respectively at the 15th SCLK falling edge. From the next falling edge, the conversion results are successively output, and LSBs are output at the 26th-SCLK falling edge. If CS low continues, SDO1 and SDO2 output "0" from the 27th-SCLK falling edge to the CS rising edge. The conversion frame ends at the CS rising edge, and SDO1 and SDO2 become Hi-Z.

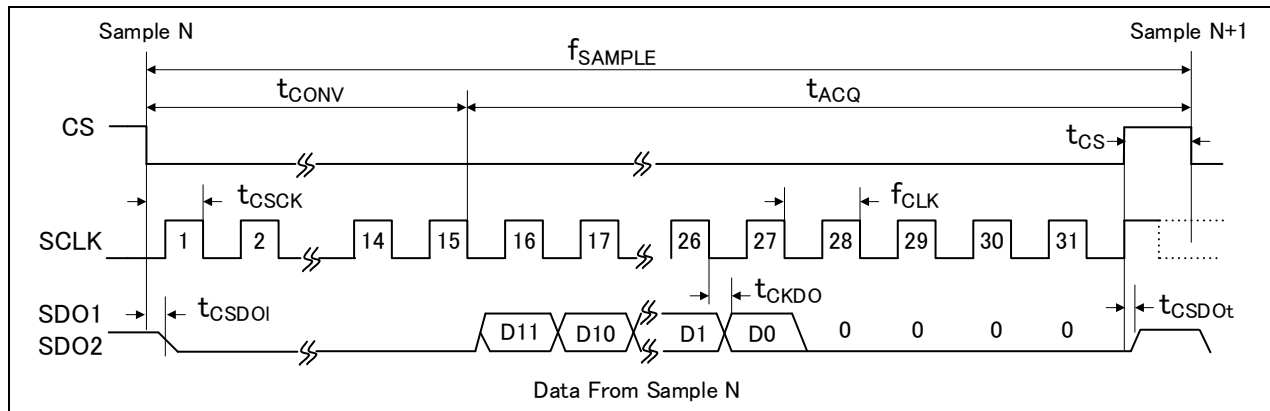


Fig. 2 Analog to digital conversion timing

Short cycle read

Fig. 3 shows a short cycle read timing diagram. Sampled input analog values are converted to digital values during 15 CLKs. From the 15th SCLK falling edge, the conversion results are successively output to SDO1 and SDO2 in MSB first order. If the CS is made high before the 26th SCLK falls, the successive outputs from SDO1 and SDO2 will be Hi-Z.

The output data from SDO1 and SDO2 before the CS is made high is valid. In some cases, CS high period must be kept after conversion abort to set aside enough time to collect analog signals until the next conversion frame.

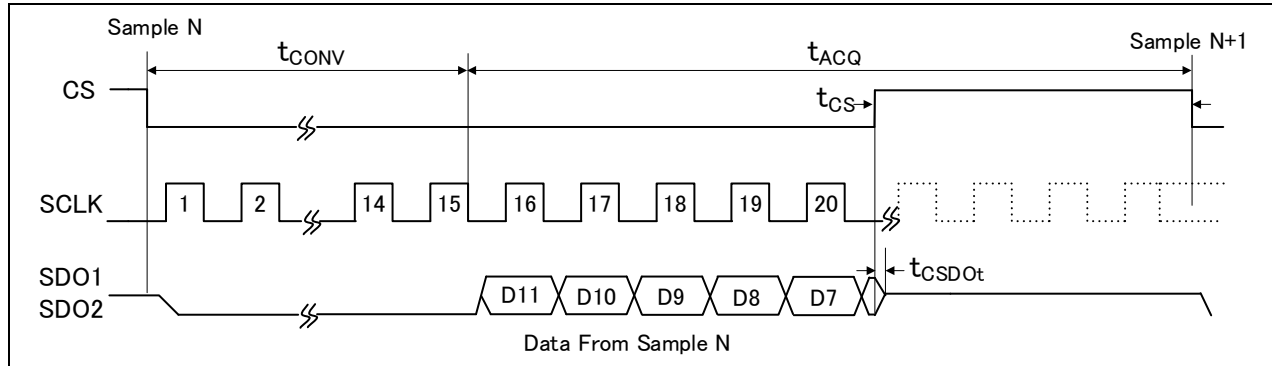


Fig. 3 Short cycle read

Conversion abort, Reconversion, Power-on

When CS is changed to high before the 15th SCLK falls, the conversion is aborted and sampling of the next analog input signal is started (Fig. 4). CS high period must be kept after conversion abort to set aside enough time to collect analog signals until the next conversion frame. Additionally, abnormal data may be output due to lack of the time to collect analog signals for the first conversion because this IC is reset at the first CS rising edge when the power is turned on. In this case, the initial data should be discarded.

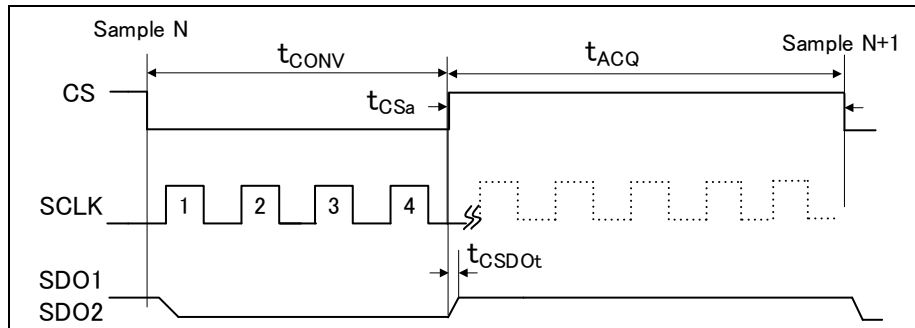


Fig. 4 Conversion abort

ANALOG INPUT

MM3804A12 supports pseudo-differential input of analog signals. There are two channels of analog input and simultaneous sampling is possible. Fig. 5 shows an equivalent circuit of analog input. A diode is connected to pins for ESD protection.

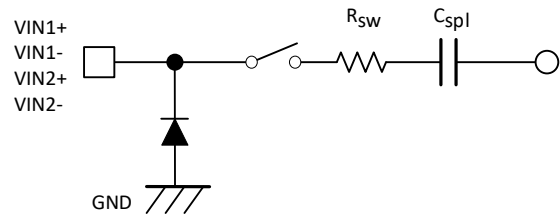


Fig. 5 Equivalent analog input circuit

DATA FORMAT

The data output from SDO1 and SDO2 is in two's complement binary format. Table 1 shows analog input voltage and ideal output codes.

Table 1 Differential analog input voltage and ideal output codes

State	Input voltage		Pseudo differential input voltage (VIN*+) - (VIN*-)	Output code	
	VIN*-	VIN*+		BIN	HEX
+Full scale	VREF*	2×VREF* - 1LSB	VREF* - 1LSB	0111 1111 1111	7FF
Middle scale		VREF*	0	0000 0000 0000	000
Middle scale - 1LSB		VREF* - 1LSB	-1LSB	1111 1111 1111	FFF
1LSB		1LSB	-VREF* + 1LSB	1000 0000 0001	801
-Full scale		0	-VREF*	1000 0000 0000	800

VIN*+, VIN*-, VREF*:VIN1+, VIN1-, VREF1 or VIN2+, VIN2-, VREF2
1LSB=FSR/2¹²=FSR/4096
VREF* equal to 2.5V, 1LSB is 1.22mV

TYPICAL APPLICATION CIRCUIT

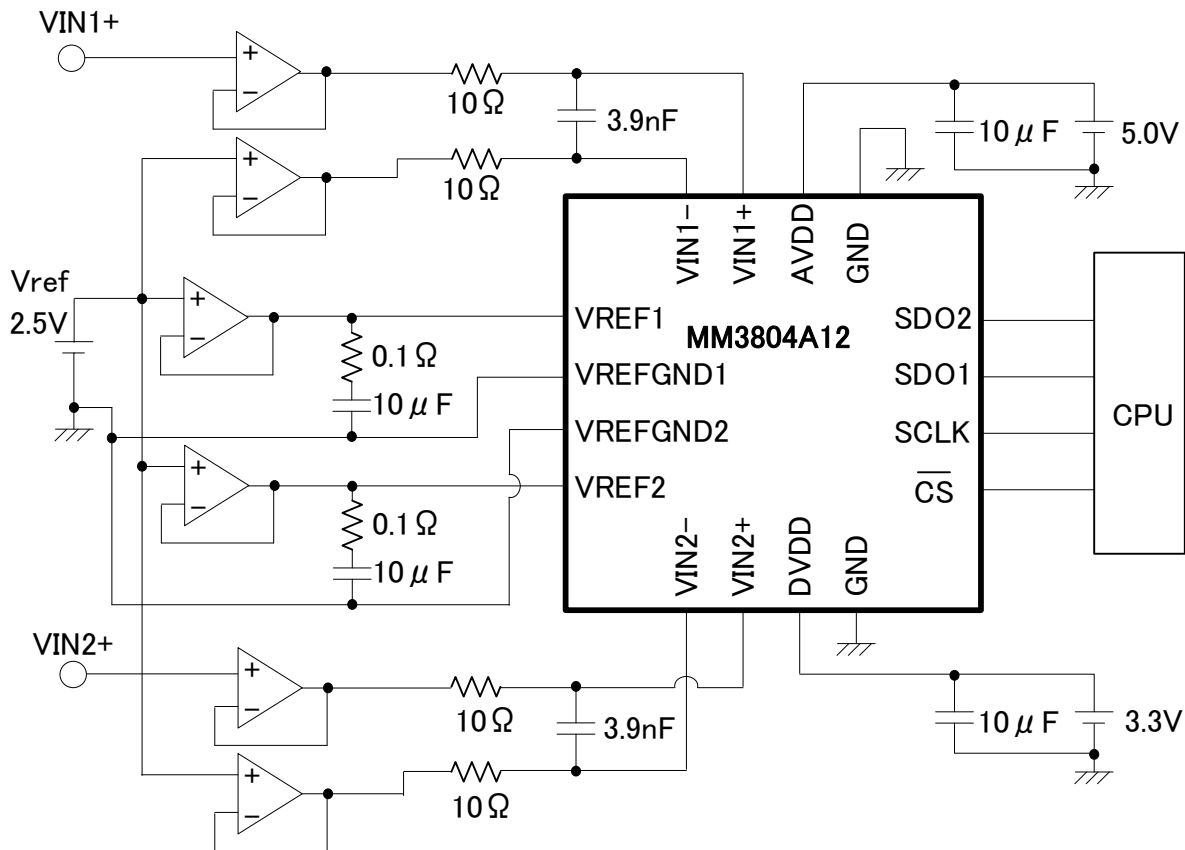


Fig. 6 Typical application circuit for 10KHz input signal at 750Ksps

APPLICATION HINTS

- A ceramic capacitor of 1μF to 10μF must be connected near AVDD and DVDD, respectively. This improves voltage ripple and resistance to external noises, and stabilizes the system.
- VREF1 and VREFGND1 pins must be separated from VREF2 and VREFGND2 pins. A resistor of 0.1Ω must be connected to the ceramic capacitor of 1μF to 10μF in series near and between VREF1 and VREFGND1 and between VREF2 and VREFGND2 for stabilization. And It is recommended the capacitance value be verified with the actual device.
- High frequency components must be removed from signals input to the analog input pin using an RC low-pass filter. The capacitor not only removes high frequency components from input signals but also reduces the sampling charge injection of the sampling capacitor in ADC. It is recommended that the filter constant be verified with the actual device.
- AVDD, DVDD, GND, VREFGND1, and VREFGND2 wires must be sufficiently strengthened because they may cause noises and unstable operations when their impedance is high.
- AVDD and GND pins and DVDD and GND pins are positioned side by side, respectively. If short circuit occurs during board mounting, peripheral devices may be destroyed.

TYPICAL PERFOR MANCE CHARACTERISTICS

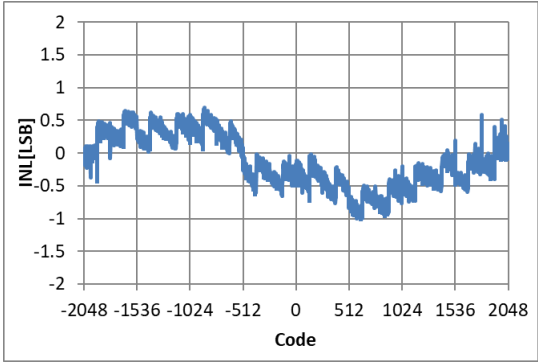


Fig. 7 INL

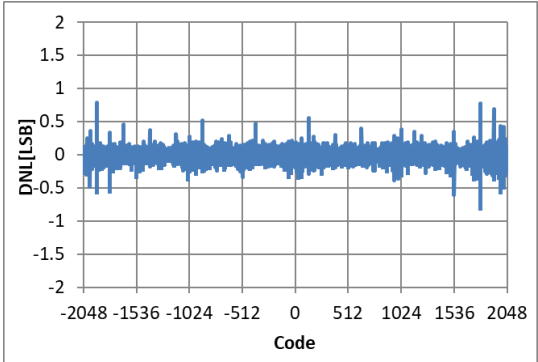


Fig. 8 DNL

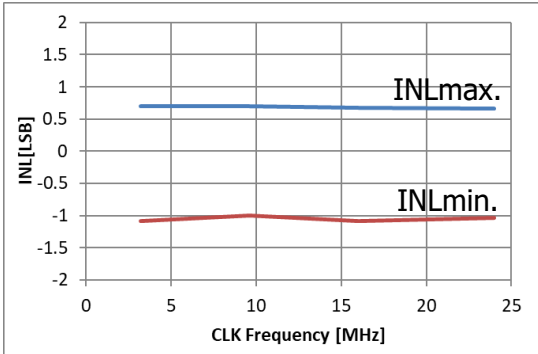


Fig. 9 INL vs SCLK Frequency

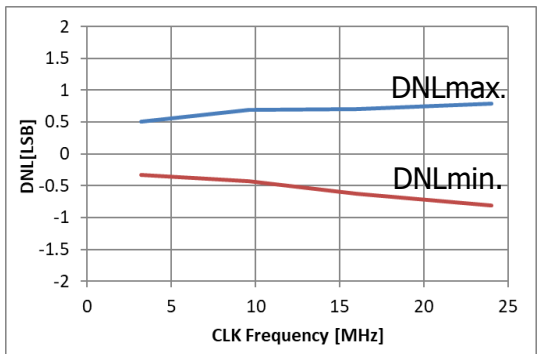


Fig. 10 DNL vs SCLK Frequency

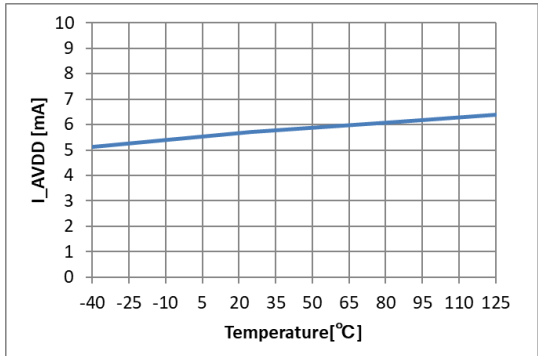


Fig. 11 Analog current (operational) vs Temperature

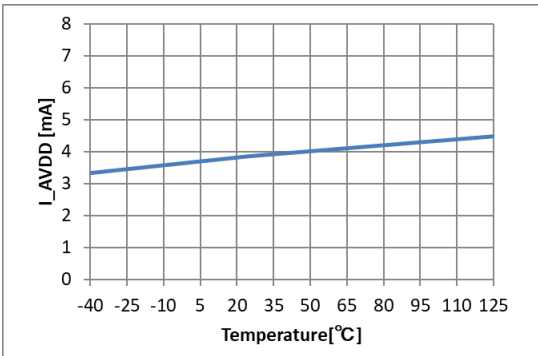


Fig. 12 Analog current (static) vs Temperature

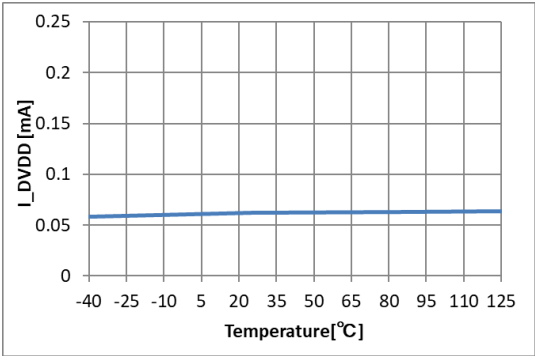
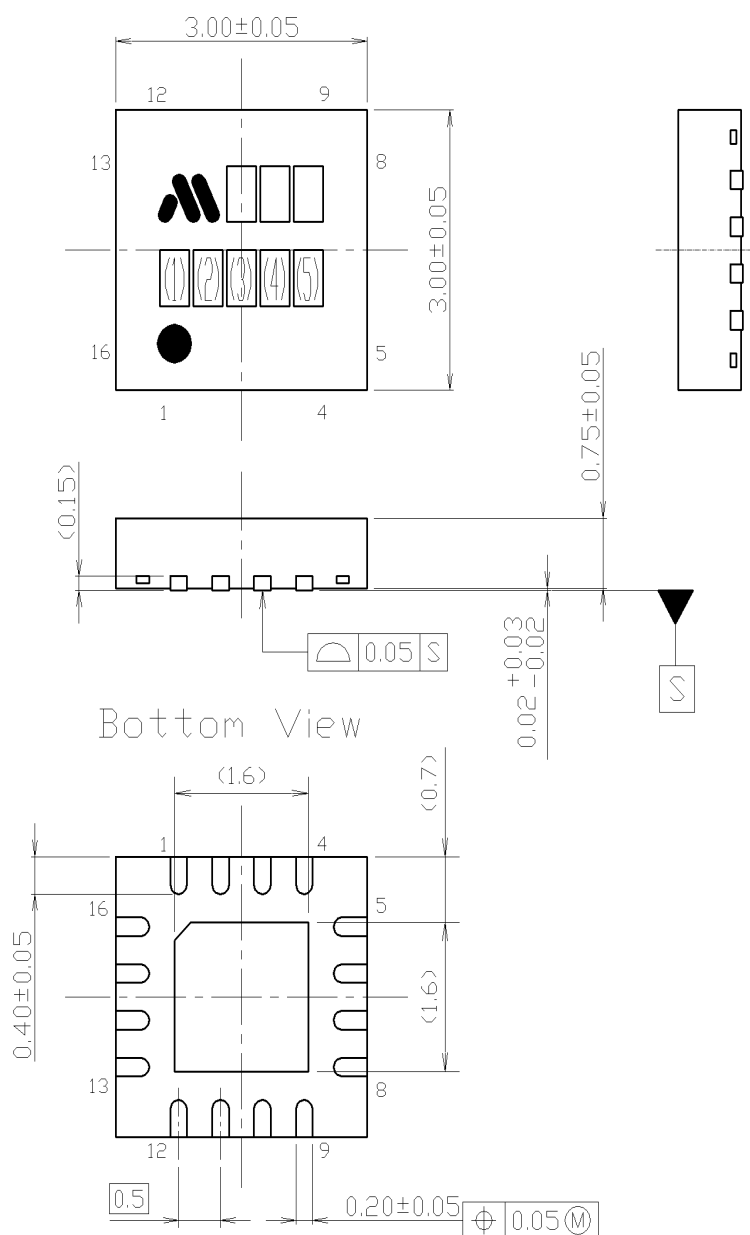


Fig. 13 Digital current vs Temperature

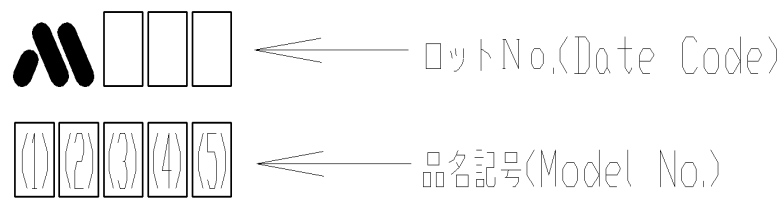
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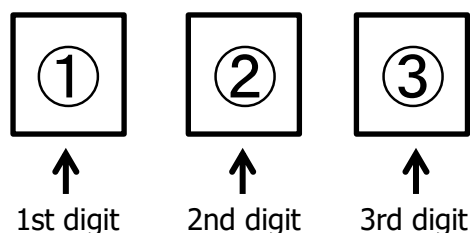
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MARKING CONTENTS



Model name	Model No.				
M M 3 8 0 4 A 1 2 R x x 8	(1)	(2)	(3)	(4)	(5)
	8	0	4	A	2

How to identify 3 characteristic lot numbers.



1. The 1st digit (①) shows the last digit of a production year (western calendar).
2. The 2nd (②) and 3rd (③) digit show a production week of mass production.

【How to indicate a production year】

The 1st digit (①)	
the last digit of a production year	mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

The 2nd and 3rd digit (②③)			
production week	mark	production week	mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53

NOTES

Safety Precautions

- Though Mitsumi Electric Co., Ltd. (hereinafter referred to as "Mitsumi") works continually to improve our product's quality and reliability, semiconductor products may generally malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of this product could cause loss of human life, bodily injury, or damage to property, including data loss or corruption. Before customers use this product, create designs including this product, or incorporate this product into their own applications, customers must also refer to and comply with (a) the latest versions or all of our relevant information, including without limitation, product specifications, data sheets and application notes for this product and (b) the user's manual, handling instructions or all relevant information for any products which is to be used, or combined with this products. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. Mitsumi assumes no liability for customers' product design or applications.
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- Before using this product, please evaluate and confirm the actual application with this product mounted and embedded.
- To investigate the influence by applied transient load or external noise, It is necessary to evaluate and confirm them with mounting this product to the actual application.
- Any usage above the maximum rating may destroy this product or shorten the lifetime. Be sure to use this product under the maximum rating.
- If you continue to use this product highly-loaded (applying high temperature, large current or high voltage; or variation of temperature) even under the absolute maximum rating and even in the operating range, the reliability of this product may decrease significantly. Please design appropriate reliability in consideration of power dissipation and voltage corresponding to the temperature and designed lifetime after confirming our individual reliability documents (such as reliability test report or estimated failure rate). It is recommended that, before using this product, you appropriately derate the maximum power dissipation (typically, 80% or less of the maximum value) considering parameters including ambient temperature, input voltage, and output current.

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 - Environment with high temperature or high humidity where dew condensation may occur
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